Notice of Allowability	Application No.	Applicant(s)	
	09/928,767	CHHOR ET AL.	
	Examiner	Art Unit	
	Jared J. Fureman	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the telephone interview on 9/23/2004*.

2. ☒ The allowed claim(s) is/are *1-12,14 and 21-27*.

3. ☒ The drawings filed on *08 December 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *092804* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Receipt is acknowledged of the amendment, filed on 6/29/2004, which has been entered in the file.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Kevin L. Daffer (34,146) on 9/23/2004. During the interview, Mr. Daffer authorized an examiner's amendment to claims 1, 4, 8, 10-13 and 21, in order to clarify that all the conductors extend in a single direction or terminate in a single direction, incorporate the stacked integrated circuits limitation of claim 13 into claim 1, and clarify that the stacked integrated circuits are directly connected to the first end of the plurality of conductors. Following the examiner's amendment, claims 1-12, 14, and 21-27 are in condition for allowance.

The application has been amended as follows:

In the claims:

1. (Currently amended) A memory module, comprising:

a plurality of conductors, each of which have opposed first and second ends;

~~an integrated circuit coupled~~ a stacked pair of integrated circuits connected directly to the first end of each of the plurality of conductors; and

a molded resin encasing the stacked integrated ~~circuit~~ circuits and having a first outer planar surface along which a lateral surface of the plurality of conductors partially extends to the respective second ends so that all conductors terminate in a single row substantially flush with a second outer planar surface approximately perpendicular to the first outer surface.

2. (Previously presented) The memory module as recited in claim 1, wherein an edge of the memory module is adapted for slideable engagement into a receptor that is electrically connected to an electronic system.

3. (Original) The memory module as recited in claim 2, wherein the second end of each of the plurality of conductors are adapted for frictional engagement with, and electrical connection to, conductive elements arranged within the receptors, during times when the edge of the memory module is slid into the receptor.

4. (Currently amended) The memory module as recited in claim 1, wherein the molded resin extends at least partially around the stacked integrated ~~circuit~~ circuits to form an entire outer dimension of the memory module.

5. (Original) The memory module as recited in claim 4, wherein the entire outer dimension of the memory module is of equivalent size to a memory card.

6. (Previously presented) The memory module as recited in claim 4, wherein the memory module is mechanically and electrically interchangeable with a memory card.

7. (Original) The memory module as recited in claim 4, wherein the entire outer dimension of the memory module except for the second end of each of the plurality of conductors is surrounded by a covering that employs a mechanical tab which, when actuated, prevents writing data to the integrated circuit.

8. (Currently amended) The memory module as recited in claim 4, wherein a surface of the stacked integrated ~~circuit~~ circuits is bonded to a surface of a conductive plate, the opposite surface of the conductive plate extends flush with or beyond the outer dimension of the memory module.

9. (Original) The memory module as recited in claim 8, wherein the plate is thermally conductive.

10. (Currently amended) The memory module as recited in claim 1, wherein the stacked integrated ~~circuit~~ circuits comprises memory and a memory controller embodied upon a single monolithic silicon substrate.

11. (Currently amended) The memory module as recited in claim 1, further comprising wires extending between a plurality of bonding pads on the stacked integrated ~~circuit~~ circuits and the first end of each of the plurality of conductors.

12. (Currently amended) The memory module as recited in claim 1, further comprising solder extending between a plurality of bonding pads on the stacked integrated ~~circuit~~ circuits and the first end of each of the plurality of conductors.

13. (Canceled)

14. (Original) The memory module as recited in claim 1, wherein the plurality of conductors comprise flattened metal strips attributed to lead frame or a tape mounted upon a Tape Automated Bonding (TAB) device.

15-20. (Canceled).

21. (Currently amended) A method for forming a memory module, comprising:

coupling an integrated circuit to at least one of a plurality of conductors all ~~of which extend~~ conductors extending substantially parallel to each other and in a single direction laterally from the integrated circuit along two planes substantially parallel with a plane formed by the integrated circuit;

securing the plurality of conductors between a pair of mold housings, each of which have a cavity that surrounds opposed surfaces of the integrated circuit absent any structure between the coupled integrated circuit and the pair of mold housings; and

inserting resin between the pair of mold housings.

22. (Original) The method as recited in claim 21, wherein said coupling comprises ultrasonic or thermosonic bonding a wire between the integrated circuit and said at least one of the plurality of conductors.

23. (Original) The method as recited in claim 21, wherein said coupling comprises Tape Automated Bonding (TAB) said at least one of the plurality of conductors to at least one bonding pad upon the integrated circuit.

24. (Original) The method as recited in claim 21, wherein said coupling further comprises mounting another integrated circuit offset upon an upper surface of the

integrated circuit to expose a set of bonding pads on the integrated circuit to the plurality of conductors.

25. (Original) The method as recited in claim 24, wherein said mounting further comprises coupling said another integrated circuit to at least one of the plurality of conductors.

26. (Original) The method as recited in claim 21, wherein said securing comprises suspending the integrated circuit within an air-filled space formed by the cavity of each of the mold housings by clamping the plurality of conductors between the pair of mold housings a spaced distance from the cavity.

27. (Original) The method as recited in claim 21, wherein said inserting resin comprises flowing the resin in liquid form into an air-filled space formed by the cavity of each of the mold housings and then allowing the resin to harden.

Allowable Subject Matter

2. Claims 1-12, 14, and 21-27 have been allowed over the prior art of record.

3. The following is an examiner's statement of reasons for allowance: The prior art of record, taken alone or in combination, fails to teach or fairly suggest a memory module including a stacked pair of integrated circuits connected directly to a first end of a plurality of conductors with molded resin encasing the stacked integrated circuits

having a first outer planar surface along which a lateral surface of the plurality of conductors partially extending to respective second ends so that all conductors terminate in a single row substantially flush with a second outer planar surface approximately perpendicular to the first outer surface; and a method for forming a memory module comprising coupling an integrated circuit to at least one of a plurality of conductors, all conductors extending substantially parallel to each other and in a single direction laterally from the integrated circuit and securing the plurality of conductors between a pair of mold housings, each of which have a cavity that surrounds opposed surfaces of the integrated circuit absent any structure between the coupled integrated circuit and the pair of mold housings; in combination with the other claimed limitations as set forth in the claims.

While Eskildsen et al (US 6,704,204) teaches a memory module (40, see figure 5) including a plurality of conductors (44), an integrated circuit (not shown) connected to a first end of the plurality of conductors and a molded resin (42) encasing the integrated circuit and having a first outer planar surface (a top surface of support 46) along which a lateral surface of the plurality of conductors partially extends to respective second ends so that all conductors terminate in a single row substantially flush with a second outer planar surface (a side surface of support 46) approximately perpendicular to the first outer planar surface, Eskildsen et al fails to teach a stacked pair of integrated circuits connected directly to the first end of each of the plurality of conductors.

Liu (US 6,316,727) and Akram (US 6,297,547) both teach stacked integrated circuits directly connected to a conductor. However both references fail to teach all

conductors terminating in a single row, the references teach conductors terminating in two rows, and the conductors extending past a casing.

Takiar et al (US 5,422,435) and Farnworth (US 5,012,323) both teach stacked integrated circuits connected directly to conductors having second ends that terminate in a single row. However, neither reference teaches a molded resin encasing the stacked integrated circuits having a first outer planar surface along which a lateral surface of the plurality of conductors partially extending to respective second ends so that all conductors terminate in a single row substantially flush with a second outer planar surface approximately perpendicular to the first outer surface.

Nishizawa et al also teaches stacked integrated circuits (see figure 5), however the stacked integrated circuits 34a and 34b are connected to bonding patterns 39, and are not directly connected to a first end of conductors which partially extend along a first outer planar surface of a molded resin encasing the integrated circuits and having a second end that terminates substantially flush with a second outer planar surface approximately perpendicular to the first outer surface.

While the individual features of applicant's invention are taught by the prior art of record, without the benefit of applicant's teachings, there is no motivation for one of ordinary skill in the art at the time of the invention to combine each of the certain specific features from the prior art of record in a manner so as to create the claimed invention.

Furthermore, applicant's argument, see the second full paragraph on page 10 of the amendment filed on 6/29/2004, have been considered and are persuasive. Since

Iwasaki '912 teaches the memory module having conductors that extend in two directions laterally from the integrated circuit, Iwasaki '912 does not suggest securing the plurality of conductors, wherein all conductors extend in a single direction laterally from the integrated circuit, between a pair of mold housings each of which have a cavity that surrounds opposed surfaces of the integrated circuit absent any structure between the coupled integrated circuit and the pair of mold housings, in combination with the other claimed limitations as set forth in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eskildsen et al (US 6,704,204), Boon et al (US 2004/0084741), Osaka et al (US 2004/0066693), Yamamoto (US 6,733,954), Verma et al (US 6,731,011), Nakoaka et al (US 6,583,512), Huang et al (US 6,414,385), Wehrly, Jr. (US 2004/0183206), Abe et al (US 2004/0178490), Verma (US 6,731,011), Verma et al (US 2004/0169285), Liu (US 6,316,727), Takiar et al (US 5,422,435), Akram (US 6,297,547), Farnworth (US 5,012,323) and Casto (US 5,172,214) all teach memory modules and/or methods for making memory modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared J. Fureman whose telephone number is (571)

272-2391. The examiner can normally be reached on 7:00 am - 4:30 PM M-T, and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared J. Fureman
Examiner
Art Unit 2876

September 28, 2004